We claim:

1. A method for transmission of transmission or received data between two adjacent, series-connected modules in a transmission/reception path of a device for production and processing of data bursts, which is contained in a device for transmission and reception of data without the use of wires, the method comprising the steps of:

- when transmission data is being transmitted without the use of wires, the two modules are a part of the transmission path, and transmission data is transmitted from a first of the two modules to a second of the two modules, information relating to the validity of the transmission data is transmitted from the first module to the second module, and information relating to the reception of valid transmission data is transmitted from the second module to the first module, and
- when received data is received without the use of wires, the two modules are a part of the reception path, and received data is transmitted from the second module to the first module, information relating to the validity of the received data is transmitted from the second module to the first module, and information relating to the reception of valid received data is transmitted from the first module to the second module.

2. The method as claimed in claim 1, wherein

- information relating to the completion of a data transmission, in particular relating to the completion of the transmission of a data packet, is transmitted from the first module to the second module during transmission, and is transmitted from the second module to the first module during reception.

3. The method as claimed in claim 1, wherein
- the first module and the second module are connected to one another by means of hard wiring, in which connections for data and information transmission between the first module and the second module are defined by software which, for this purpose, in particular sets registers.

4. The method as claimed in claim 1, wherein
- a clock transmitter unit produces a clock signal which, in particular, is at a clock rate of 26 MHz.

5. The method as claimed in claim 4, wherein
- the transmission of data and/or information starts and ends with a clock signal from the clock transmitter unit.

6. The method as claimed in claim 4, wherein
- the clock signal is a binary square-wave signal.

7. The method as claimed in claim 6, wherein
- the transmission of data and/or information starts and ends with a change in the binary square-wave signal from a bit0 state to a bit1 state, or from a bit1 state to a bit0 state.

8. The method as claimed in claim 1, wherein
- the data comprises bit strings.

9. The method as claimed in claim 1, wherein
- the information relating to the validity of the data and/or the information relating to the reception of valid data and/or the information relating to the completion of a data transmission have/has binary states.

10. The method as claimed in claim 9, wherein
- during the transmission of valid data, the information relating to the validity of the data is transmitted in a bit1 state or in a bit0 state.

11. The method as claimed in claim 10, wherein
- when one of the modules receives data and when the module receives information relating to the validity of the data in a high state, a pulse is transmitted in a bit1 state or in a bit0 state as information relating to the reception of valid data from the module.

12. The method as claimed in claim 9, wherein
- after the completion of the transmission of data by one of the modules and after the valid reception of the data by the respective module other than the transmitting module, the information relating to the completion of a data transmission is sent in a bit1 state or in a bit0 state.

13. The method as claimed in claim 1, wherein
- the at least two series-connected modules can be selected from the totality of a list of modules which comprises the following modules:
  - a module for access to a memory unit,
  - a module with a CVSD coder and/or CVSD decoder,
  - a module with an ADPCM unit,
  - a module with a CRC generator and/or a CRC processor,
  - a module for scrambling and/or descrambling of data,
  - a module with a scrambler and/or descrambler,
  - a module with an FEC unit,
  - a module with a FIFO memory, and
  - a module with a unit for transmission and/or for reception of data, with
- the selected modules being integrated in particular on a common fixed substrate.